Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, APRIL – MAY 2025

Third Semester

Artificial Intelligence and Data Science

CS3351 – Digital Principles and Computer Organization

(Common to Computer Science and Engineering & Information Technology)

Regulations - 2021

Duration : 3 Hrs ***Maximum : 100 Marks***

PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	Write the design procedure for combinational circuits.	L2	1	2
2.	Design a 1-bit Magnitude Comparator.	L2	1	2
3.	Write the difference between Combinational and Sequential Circuits.	L2	2	2
4.	Mention the different types of shift registers.	L1	2	2
5.	Specify the registers generally contained in the processor.	L2	3	2
6.	List the phases, which are included in each instruction cycle.	L1	3	2
7.	When will the instruction have a die effect?	L2	4	2
8.	Define branch folding and write the conditions for implementing it.	L1	4	2
9.	When does the write stall occur?	L1	5	2
10.	Define Page Fault.	L1	5	2

PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a		With a neat sketch elaborate on the functionality of the full adder and demonstrate how it can be used to add two binary numbers.	L3	1	16
			Or			
	b		Define K-map. Simplify the Boolean function F(w,x,y,z)=∑(0,1,2,4,5,6,8,9,12,13,14) using K-map.	L3	1	16
12.	a	i	Realize D Flip flop using SR Flip flop.	L4	2	8
		ii	Analyze the design of D Flip flop with two D Latches and an inverter with a neat diagram.	L4	2	8
			Or			
	b		Illustrate Mealy and Moore Models with block diagrams.	L2	2	16
13.	a		Outline the Von Neumann architecture with a neat diagram.	L2	3	16
			Or			
	b		Define Addressing Mode. Outline the types of addressing modes with examples.	L2	3	16

14.	a	Depict how instruction is being fetched and executed through the data path in the processor.	L2	4	16
		Or			
	b	Describe data hazards and control hazards. Explain with suitable techniques, how these hazards are mitigated.	L2	4	16
15.	a	Illustrate the various memory mapping techniques for finding the memory blocks in the cache with example.	L2	5	16
		Or			
	b	Elaborate how virtual address is translated to physical address? Explain it with the help of virtual memory organization and page translation.	L2	5	16